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Patent Application Transmittal Letter

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Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility () Design
(X) original patent application,
() continuation-in-part application

INVENTOR(S): Samuel D. Naffziger

TITLE: Static To Dynamic Logic Interface Circuit

Enclosed are:

- (X) The Declaration and Power of Attorney. (X) signed () unsigned or partially signed
(X) 1 sheets of drawings (one set) () Associate Power of Attorney
() Form PTO-1449 () Information Disclosure Statement and Form PTO-1449
() Priority document(s) () (Other) (fee \$)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	16 — 20	0	X \$18	\$ 0
INDEPENDENT CLAIMS	4 — 3	1	X \$80	\$ 80
ANY MULTIPLE DEPENDENT CLAIMS	0		\$270	\$ 0
BASIC FEE: Design (\$320.00); Utility (\$710.00)				\$ 710
TOTAL FILING FEE				\$ 790
OTHER FEES				\$
TOTAL CHARGES TO DEPOSIT ACCOUNT				\$ 790

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By Peggy Oyama
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Respectfully submitted,

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STATIC TO DYNAMIC LOGIC INTERFACE CIRCUIT

FIELD OF THE INVENTION

The present invention relates generally to CMOS integrated circuits, and more particularly, to CMOS circuit techniques for interfacing from static single-ended logic to differential dynamic logic.

BACKGROUND OF THE INVENTION

Static logic gates have been utilized to construct logic circuits for performing mathematical operations. Static logic gates are those which can continuously perform logic operations so long as electrical power is available. In other words, static logic gates need no electrical precharge, or refresh, in order to properly perform logic operations. However, static logic gates are undesirably slow individually and, when chained together to collectively perform a logic function, are even slower.

Dynamic logic gates are used in the design of logic circuits which require high performance and modest size. Dynamic logic gates are those which require a periodic electrical precharge, or refresh, such as with a dynamic random access memory (DRAM), in order to maintain and properly perform its intended logic function. Once an electrical precharge supplied to a dynamic logic gate has been discharged by the dynamic logic gate, the dynamic logic gate can no longer perform

another logic function until subsequently precharged. Accordingly, dynamic logic usually has at least two clock phases. One clock phase is called the precharge phase. During the precharge phase, the electrical precharge is supplied to the dynamic logic gates. A second clock phase is called the evaluate phase. During the evaluate phase,
5 the electrical precharges of the dynamic logic gates may be discharged depending upon the inputs to the dynamic logic gates.

It is often desirable to mix static and dynamic logic circuits on the same integrated circuit. This allows the designer to pick the appropriate type of logic depending upon a variety of factors including speed, power dissipation, simplicity,
10 cost, and ease of use.

Unfortunately, a typical requirement of dynamic logic is that the inputs to a dynamic gate either remain stable during the entire evaluate phase, or that the inputs are monotonic. That means that only one transition from a predetermined logic level to the other one may occur without causing problems. Typically, the allowed
15 transition is a single low to high transition. However, static logic may transition in either direction, multiple times, during a clock cycle. Therefore, signals driven by static logic should not be used as inputs to dynamic logic. This presents a problem for integrated circuits that want to mix static and dynamic logic circuits.

Accordingly, there is a need in the art for a circuit that interfaces static logic to
20 dynamic logic. It is desirable that such a circuit use clocks that are standard to both the static and dynamic circuits. This simplifies design. Likewise, to simplify design, such a circuit should use standard circuit elements.

SUMMARY OF THE INVENTION

In a preferred embodiment, the invention provides a static logic signal to dynamic logic interface that produces a monotonic output. The invention is fast because it does not introduce a "dead" gate delay where no useful logic function is performed into the evaluation phase of the dynamic logic. The invention does not require the generation of special clocks that can create setup and hold time problems. Finally, the invention may be constructed using standard CMOS integrated circuit building blocks which simplifies design and implementation.

An embodiment of the invention uses standard clock signals, a delay element that can be as simple as a series of inverters, and an enabled latch to interface static logic to dynamic logic. The inverse of the dynamic logic evaluate clock is fed to the clock input of a transparent latch with clock and enable inputs. A delayed version of this clock is generated by the delay element. This delayed inverse of the dynamic logic evaluate clock is fed to the enable input of the latch. The input to the latch comes from static logic and the output of the latch is fed to the dynamic logic. The net result is a latch that is open until the evaluate clock is instructing the dynamic logic to reset, or precharge, and remains closed until a delay element delay time after the evaluate clock instructs the dynamic logic to reset.

Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration of a static logic to dynamic logic interface that produces a monotonic output.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic illustration of a static to dynamic logic interface that produces a monotonic output. In FIG. 1, IN is the input signal from static logic. OUT is the output signal that may be connected to dynamic logic. CK is the dynamic logic evaluate clock. In the embodiment shown in FIG. 1, when CK is high it is the dynamic logic evaluate phase. CK is input to delay element 104. The output of delay element is a delayed version of CK called CKD. Delay element 104 may be as simple as an even number of inverters. CK is also connected to the clock input of a transparent latch 102 and CKD is connected to an enable input of transparent latch 102.

The net result of feeding CK and CKD the clock input and the enable input, respectively, of transparent latch 102 is a static to dynamic logic interface that is open until the inverse of the dynamic logic evaluate clock rises. This static to dynamic logic interface also remains closed until a delay element delay after the dynamic logic evaluate clock falls. These properties help prevent hold time problems while providing timing benefits in an easy to construct solution with low implementation cost.

In FIG. 1, static logic signal IN is connected to the source of n-channel MOSFET (NFET) 138 and the source of p-channel MOSFET (PFET) 134. The drain of NFET 138 is connected to the source of NFET 136. The drain of NFET 136 is connected to node IN1. IN1 is a latching node for transparent latch 102 in that feedback provided by other transistors 124, 126, 132, 130, and 128 cause the value on IN1 to be retained even when pass gates 138, 136, and 134 are all off.

The drain of PFET 134 is also connected to IN1. IN1 is connected to the input of an inverter comprised of NFET 122 and PFET 120. The output of this inverter is

OUT. This arrangement allows static logic signal IN to propagate through pass gate transistors 138, 136, and 134 to IN1 and then to OUT with only one inverter gate delay plus some delay from the pass gate transistors. Accordingly, when pass gate transistors 138, 136 and 134 are on, changes in the signal IN are passed quickly to the
5 output, OUT.

Also in FIG. 1, the enable input of transparent latch 102 which is connected to CKD, is connected to the gate of NFET 138, the gate of NFET 146, and the gate of PFET 140. The clock input of transparent latch 102 which is connected to CK, is connected to the gate of NFET 136, the gate of NFET 144, and the gate of PFET 142.
10 The source of NFET 146 is connected to the negative supply voltage. The drain of NFET 146 is connected to the source of NFET 144. The drain of NFET 144 is connected to node NPCK. Node NPCK is connected to the drain of PFETs 140 and 142. NPCK is also connected to the gate of PFET 134 and the gate of NFET 130.

As mentioned above, NFET 122 and PFET 120 are connected to form an
15 inverter. Accordingly, node IN1 is connected to the gate of NFET 122 and the gate of PFET 120. The drain of NFET 122 and the drain of PFET 120 are connected to node OUT. The source of NFET 122 is connected to the negative supply voltage. The source of PFET 120 is connected to the positive supply voltage.

Node IN1 is also connected to an inverter constructed with NFET 126 and
20 PFET 124. Accordingly, node IN1 is connected to the gate of NFET 126 and the gate of PFET 124. The drain of NFET 126 and the drain of PFET 124 are connected to node FB. The source of NFET 126 is connected to the negative supply voltage. The source of PFET 124 is connected to the positive supply voltage.

Node FB is connected to the gate of PFET 132 and the gate of NFET 128.
25 The source of NFET 128 is connected to the negative supply voltage. The drain of

NFET 128 is connected to the source of NFET 130. The drain of NFET 130 is connected to node IN1. The drain of PFET 132 is also connected to node IN1.

From the foregoing it will be appreciated that the static to dynamic logic interface provided by the invention offers numerous advantages. It may be

5 constructed from elements common to many integrated circuit designs. It uses a standard clock signal as an input clock. Finally, the various delays from its inputs to its output help prevent hold time problems while providing timing benefits.

Although a specific embodiment of the invention has been described and illustrated, the invention is not to be limited to the specific forms or arrangements of

10 parts so described and illustrated. The invention is limited only by the claims.

004207-10126560

CLAIMS

What is claimed is:

1. A static logic to dynamic logic interface, comprising:

a delay having a delay input and a delay output; and,

5 a latch having a clock input, an enable input, a data input for connection to static logic, and a data output for connection to dynamic logic and wherein said delay input and said clock input connect to an inverse of a dynamic logic evaluate clock and said delay output connects to said enable input.

10 2. The static logic to dynamic logic interface of claim 1 wherein said delay is comprised of a plurality of inverters.

15 3. The static logic to dynamic logic interface of claim 1 wherein said latch is a transparent latch.

20 4. The static logic to dynamic logic interface of claim 1 wherein said delay is comprised of a plurality of inverters and said latch is a transparent latch.

5. A method of interfacing static logic and dynamic logic, comprising:
supplying a static logic signal to a data input of a latch having an output;
supplying said output to dynamic logic;
clocking said latch with an inverse of a dynamic logic evaluate clock; and,

enabling said latch with a delayed version of said inverse of said dynamic logic evaluate clock.

6. The method of claim 5 wherein said latch is a transparent latch.

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7. The method of claim 5 wherein said delayed version of said inverse of said dynamic logic evaluate clock is generated by supplying a delay element with said said inverse of said dynamic logic evaluate clock.

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8. The method of claim 7 wherein said delay element is comprised of a plurality of inverters.

9. A static logic to dynamic logic interface, comprising:

a clock that is the inverse of a second clock that causes dynamic logic to evaluate;

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a delay element that generates a delayed clock; and,

a latch having a clock input that receives said clock, an enable input that receives said delayed clock, a data input that interfaces to static logic, and an output that interfaces to dynamic logic.

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10. The interface of claim 9 wherein said latch comprises:

a first pass gate having a first pass gate output, said first pass gate receiving said data input and being controlled by said delayed clock; and,

a second pass gate having a second pass gate output that controls a latching node of said latch, said second pass gate receiving said first pass gate output and being controlled by said clock.

5 11. The interface of claim 11 wherein said latch inverts said latching node of said latch to produce said output.

12. The interface of claim 11 wherein said delay element comprises a plurality of inverters.

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13. An interface for producing a monotonic signal for use by dynamic logic from a static logic signal, comprising:

a delay element; and,

a latch with an enable input, a clock input, a data input, and an output that produces said monotonic signal wherein said clock input is connected to a delay element input and said enable input is connected to a delay element output.

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14. The interface of claim 13 wherein said latch is open until said clock input falls and said latch remains closed until a delay element delay after said clock input rises.

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15. The interface of claim 14 wherein said clock input is coupled to an inverse of a dynamic logic evaluate clock.

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16. The interface of claim 15 wherein said delay element is comprised of at least one inverter.

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ABSTRACT

A static logic signal to dynamic logic interface that produces a monotonic output. An inverse of a dynamic logic evaluate clock is fed to the clock input of a transparent latch with clock and enable inputs. A delayed version of the inverse of the evaluate clock is generated by a delay element. The delayed inverse of the evaluate clock is fed to the enable input of the latch. The input to the latch comes from static logic and the output of the latch is fed to the dynamic logic. The net result is a latch that is open until the evaluate clock is instructing the dynamic logic to reset, and remains closed until a delay element delay time after the evaluate clock instructs the dynamic logic to reset.

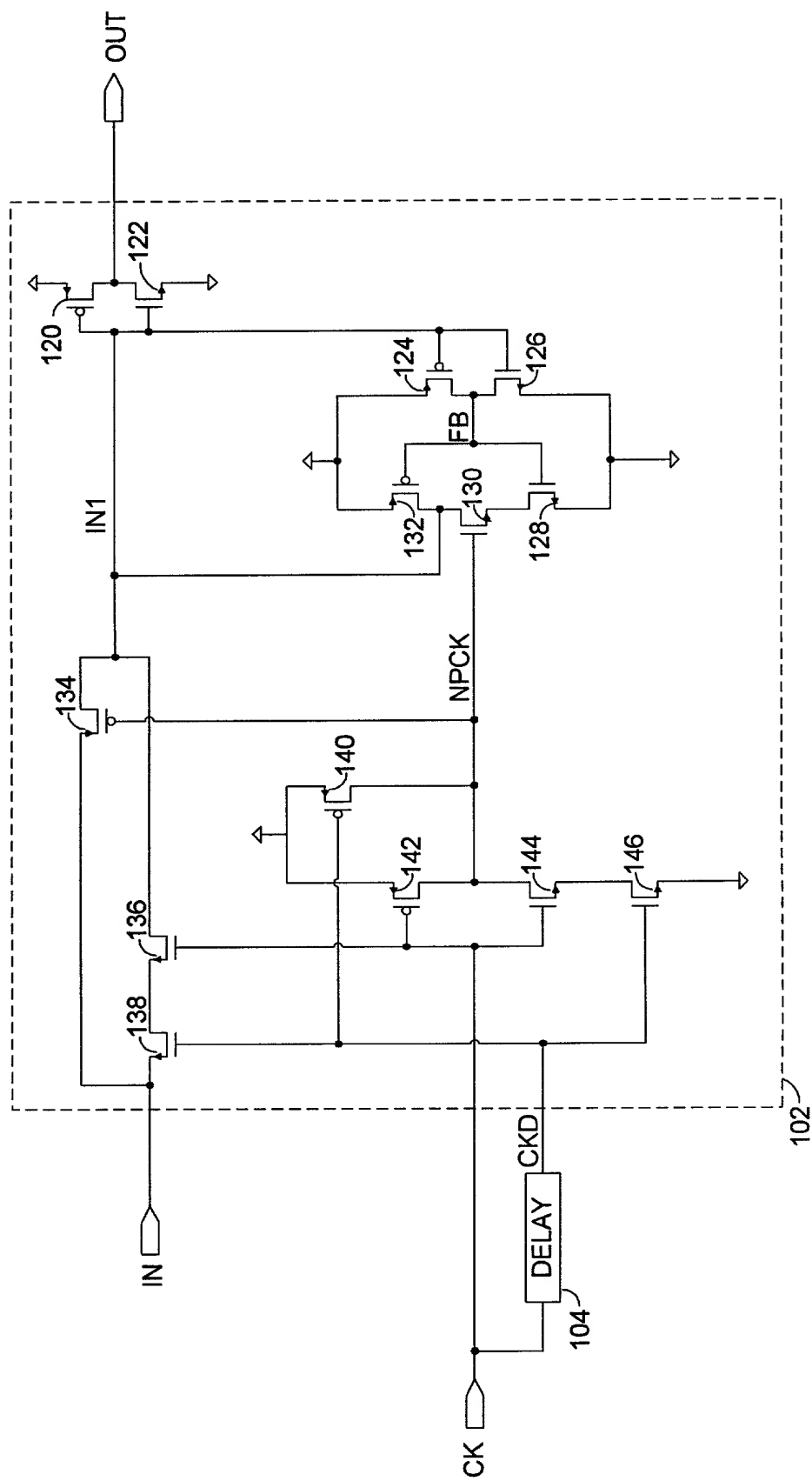


FIG. 1

**DECLARATION AND POWER OF ATTORNEY
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As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Static To Dynamic Logic Interface Circuit

the specification of which is attached hereto unless the following box is checked:

() was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
N/A			YES: _____ NO: _____
			YES: _____ NO: _____

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE
N/A	

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)
N/A		

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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